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TITLE: **Semiconductor** element e.g. integrated circuit chip used in liquid crystal display, has pillar-type **elliptical bumps** whose narrowed edges face periphery of **semiconductor** element

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ABSTRACTED-PUB-NO: JP2001358165A

BASIC-ABSTRACT:

NOVELTY - The pillar-type **elliptical bumps** (B1) are mounted in a substrate such that the narrowed edges (R1) face the periphery of **semiconductor** element.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for liquid crystal display.

USE - Integrated circuit (IC) chip, LSI chip used in liquid crystal display (LCD) (claimed), computer, etc.

ADVANTAGE - The bumps are arranged uniformly, so that the paste-like material flows in the direction of periphery smoothly, without the generation of air bubbles.

DESCRIPTION OF DRAWING(S) - The figure shows the top view of the **semiconductor** element and perspective view of the bump.

Pillar-type **elliptical bumps** B1

Edges of bumps R1

CHOSEN-DRAWING: Dwg.1/13

TITLE-TERMS: **SEMICONDUCTOR** ELEMENT INTEGRATE CIRCUIT CHIP LIQUID CRYSTAL DISPLAY PILLAR TYPE **ELLIPSE BUMP** NARROW EDGE FACE PERIPHERAL **SEMICONDUCTOR** ELEMENT

DERWENT-CLASS: P81 U14

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SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N2002-292886

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the liquid crystal display with which semiconductor devices, such as IC chip and an LSI chip, and the semiconductor device of those were mounted.
[0002]
[Description of the Prior Art] Since what has the bump who is the electrode of the letter of a projection as semiconductor devices, such as IC chip and an LSI chip, is advantageous to the miniaturization of the substrate for semi-conductor mounting, modular thin-shape-izing, etc., it is mostly used on electronic equipment, such as various computers and a liquid crystal display. Many approaches, such as the approach of a pewter, gold (Au), silver (Ag), copper (Cu), lead (Pd), nickel (nickel), etc. being used, and the bump who is the electrode of this letter of a projection printing a cream-like pewter as that quality of the material, on the bump who formed with the approach by the photolithography and plating, or a photolithography and plating, and forming, and the so-called imprint bump method, exist from the former.
[0003] As an approach of mounting such a semiconductor device with a bump in a substrate by face down, various approaches are proposed from the former. The typical approach is as follows. There is the approach of 1st forming a bump the shape of a globular form and in the shape of a semi-sphere with a pewter, considering as the so-called pewter bump, making carry out melting solidification of the pewter bump by the reflow, and connecting with the electrode of a substrate first. In addition, it considers as the golden bump who formed the bump bygold, and the precoat of the pewter is carried out by plating etc. on the electrode of a substrate, and it solders by the reflow like the above-mentioned approach, and preferably, in order to secure the junction force of a semiconductor device and a substrate, there is also an approach by which the resin for the closures is enclosed.
[0004] Next, it faces 2nd mounting a semiconductor device, and the whole wearing field on a substrate is covered, a paste-like ingredient or a film-like ingredient is supplied, a semiconductor device is positioned with a wearing machine from on the, and there is a method of stiffening a paste-like ingredient etc. with heating and a pressurization means. As a paste-like ingredient or a film-like ingredient, there are anisotropy electric conduction film (Anisotropic Conductive Film:ACF), thermocompression bonding insulation hardening resin, etc.
[0005] Next, after facing mounting a semiconductor device, imprinting ingredients, such as anisotropy electric conduction film (Anisotropic Conductive Film:ACF) and electroconductive glue (conductive paste), only on the bump of a semiconductor device and stiffening [3rd] this with a heating means, the resin for the closures for securing these junction is slushed between a semiconductor device and a substrate, and there is a method of stiffening this. Although it is usual that a cross section is gold of a square-like column type (rectangular parallelepiped) or a forward circular-like column type (cylinder mold) as a bump of the 2nd approach and the 3rd approach, pewter PAMPU may be used at this tip of a golden bump, forming it in it the shape of a globular form, and in the shape of a semi-sphere (bump of multilayer structure).
[0006]
[Problem(s) to be Solved by the Invention] By the way, as for a bump array, a pitch tends to become narrow with the densification of a semiconductor device in recent years, and the further miniaturization

of the substrate for semi-conductor mounting (a bump's formation of a fine pitch). And as shown in drawing 12 and drawing 1313 , the further fine pitch-ization of the bump B who considered Bump's B array as so-called two or more arrays of an alternate configuration is progressing.

[0007] On the other hand, in mounting of the semiconductor device in a liquid crystal display, there is COG (chip on glass) mounting which connects a direct semiconductor device to the electrode terminal on a glass substrate. Although the flexible substrate made from plastics may be used instead of a glass substrate (this may be called COF (chip on flexible) and COP (chip on plastic)), it is expected that these COG mounting etc. becomes in use from now on in the field of a liquid crystal display with remarkable miniaturization and thin-shape-izing of a liquid crystal panel. Mounting of a semiconductor device IC which they are used by the anisotropy electric conduction film and electroconductive glue in COG mounting, ****ing, and has the golden bump B of the above-mentioned configuration is usual.

[0008] However, although mounted by facing mounting a semiconductor device IC in the substrate for semi-conductor mounting, and making the ingredient of the shape of the shape of a paste, such as resin for the closures which close the anisotropy electric conduction film, electroconductive glue, a semiconductor device, and a substrate, and a film intervene, it have the problem which the situation, i.e., the situation which check a fluidity, where of a paste-like ingredient etc. do not spread smoothly in the direction of a periphery of a semiconductor device IC (the direction of a lower stream of a river) produce with the above-mentioned bump B configuration.

[0009] As shown in drawing 12 , when the cross section is the semiconductor device IC of the bump B who is a square-like column type (rectangular parallelepiped), the conductive particle of the shape of a paste, a film-like ingredient, and the anisotropy electric conduction film (ACF) may incline and spread around Bump B, or air comes to be pushed in and, specifically, air bubbles K may be made. If it cools where these air bubbles K are made, a semiconductor device and a substrate are made to produce a crack by the difference in the coefficient of thermal expansion of a paste-like ingredient and air, or when especially the anisotropy electric conduction film (ACF) is used, a conductive particle will condense around air bubbles K, and the problem of making it short-circuit horizontally etc. will be induced. Moreover, when Bump B was the column type (cylinder mold) of a right round shape, as shown in drawing 13 , the bias and the situation (situation which checks a fluidity) which does not spread equally to a mounting field were produced in the direction in which breadth, such as a paste-like ingredient, becomes parallel to a bump train. When these problems consist of a case where especially Bump's B pitch is narrow, and two or more trains, the inclination is remarkable and the problem will become big.

[0010] Moreover, in COG mounting, since the substrate for semi-conductor mounting other than the above-mentioned problem was made into one substrate of a liquid crystal panel, and one, when a paste-like ingredient etc. did not spread in the direction of a periphery smoothly, it has a possibility of becoming the load stress at the time of carrying out thermocompression bonding of the semiconductor device, and the yield of a direct liquid crystal panel might be influenced.

[0011] And in the thing of a rectangular parallelepiped or a cylinder mold, while excelling in connection dependability, in fine pitch-ization of a bump of a certain thing, the limitation had produced the advantage of being easy to manufacture in a manufacture process today when a bump's fine pitch-ization is demanded.

[0012] Then, the purpose of this invention is faced mounting a semiconductor device in the substrate for semi-conductor mounting, and it is to offer the liquid crystal display with which the semiconductor device which can attain a bump's fine pitch-ization, and its semiconductor device were mounted while it secures the homogeneous broadening of smooth flow, such as a paste-like ingredient which is not made to generate air bubbles.

[0013]

[Means for Solving the Problem] In the semiconductor device which has the bump by whom the semiconductor device of this invention according to claim 1 is mounted in the substrate for semi-conductor mounting through the ingredient of the shape of the shape of a paste, and a film, the cross section is an elliptical column type or the column type which has the streamline shape of bilateral symmetry narrow in the cross section, and the above-mentioned bump is characterized by arranging the part used as narrow [these] toward the direction of a periphery of a semiconductor device.

[0014] In the semiconductor device which has the bump by whom the semiconductor device of this invention according to claim 2 is mounted in the substrate for semi-conductor mounting through the

ingredient of the shape of the shape of a paste, and a film the above-mentioned bump It is the column type of the rhombus configuration where the cross section is long and slender, or the column type which has the part from which the cross section serves as narrow by the shape of a polygon long and slender in the direction of axial symmetry and its symmetry line, and is characterized by arranging the part used as narrow [these] toward the direction of a periphery of a semiconductor device.

[0015] According to these claims 1 or invention according to claim 2, in case a semiconductor device is mounted in the substrate for semi-conductor mounting through a paste-like ingredient etc., spread in homogeneity so that a paste-like ingredient etc. may flow in the direction of a periphery of a semiconductor device, but Since the bump who has the above-mentioned configuration and directivity becomes narrow toward the direction of a periphery of a semiconductor device It is lost that the conductive particle of breadth, a paste-like ingredient, and the anisotropy electric conduction film (ACF) inclines toward homogeneity, or the air bubbles by the fluidity of a paste-like ingredient etc. being checked are generated so that a paste-like ingredient etc. may flow smoothly in the direction of a periphery of a semiconductor device. Moreover, the conventional cross section can attain a bump's fine pitch-ization as compared with the thing of a square-like column type (rectangular parallelepiped) or a forward circular-like column type (cylindrical) from the part used as narrow being arranged toward the direction of a periphery of a semiconductor device. In addition, since each a bump's cross-section configuration is axial symmetry, it can be conventionally manufactured easily also in the manufacture process of the bump by the photolithography, plating, etc.

[0016] It is characterized by for the semiconductor device of this invention according to claim 3 shifting a mutual train while said bump consists of two or more trains along the periphery edge of a semiconductor device, and being arranged alternately.

[0017] Even when according to this invention a bump shifts a mutual train and two or more arrays are carried out alternately, it will spread in homogeneity so that a paste-like ingredient etc. may flow, and will respond to the request of the formation of a fine pitch of a bump.

[0018] The liquid crystal displays with which the semiconductor device of this invention according to claim 4 was mounted are adhesives with which the ingredient of the shape of said shape of a paste and a film has conductivity, and the substrate for said semi-conductor mounting is characterized by being one substrate of the liquid crystal panel by which liquid crystal was ****(ed) between the substrates which counter, and the substrate made into one.

[0019] According to this invention, it is lost that the conductive particle of breadth and the anisotropy electric conduction film (ACF) inclines toward homogeneity, or air bubbles are generated by checking the fluidity of the anisotropy electric conduction film (ACF) so that the anisotropy electric conduction film (ACF) which is the shape of a paste and a film-like ingredient may flow smoothly in the direction of a periphery of a semiconductor device. Moreover, also in the substrate for semi-conductor mounting made into one substrate of a liquid crystal panel, and one, in case thermocompression bonding of the semiconductor device is carried out, a possibility that load stress may start a substrate also disappears.

[0020]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained, quoting a drawing. In addition, it explains in order of the gestalt of the operation of a semiconductor device which has the bump of this invention, a bump's manufacture process, COG mounting of a semiconductor device that has a bump, mounting of the general semiconductor device IC, and MCM mounting.

[0021] Two or more bumps B1 are formed in the semiconductor device IC. As gold (Au) is used and a bump B1 shows drawing 1 , one near bump array consists of single tiers along the periphery edge of a semiconductor device IC, and the bump array of the other side shifts a mutual train, and is alternately arranged while consisting of two or more trains along the periphery edge of a semiconductor device IC. The cross section of each bump's B1 configuration is an elliptical column type (gestalt of the 1st operation). That is, it is the column type which becomes bilateral symmetry with narrow toward the direction of a periphery of a semiconductor device IC. As such a bump's B1 example, like the above-mentioned elliptical one, as long as the cross section has the narrow streamline shape R1 of axial symmetry, as shown in drawing 2 , column type bump B-2 which is water drop-like is sufficient (gestalt of the 2nd operation). Furthermore, the configuration of such a bump B1 and B-2 may be the multilayer structure of an analog like the application shown in drawing 5 (a) and (b). And in order that all may wash away smoothly the shape of a paste and film-like ingredients, such as anisotropy electric

conduction film (ACF), in the direction of a periphery of a semiconductor device IC, the part used as narrow is arranged toward the direction of a periphery of a semiconductor device IC.
[0022] Moreover, as a bump's B3 configuration is shown in drawing 3 , the column type of a long and slender rhombus configuration is sufficient as the cross section (gestalt of the 3rd operation). moreover, the above -- as long as it is the column type which has the part R2 from which the cross section serves as narrow by the shape of a polygon long and slender in the direction of axial symmetry and its symmetry line like a long and slender rhombus configuration, as shown in drawing 4 , you may have the shape of a long and slender hexagon, and the other shape of a long and slender polygon (gestalt of the 4th operation). Furthermore, as such a bump B3 and B4, the configuration may be the multilayer structure of an analog like the application shown in drawing 5 (b) and (c).
[0023] (A bump's formation process) Next, the bump B1 of the gestalt of each above-mentioned implementation, B-2, B3, and the formation process of B4 are explained. Generally, many approaches, such as an approach by the photolithography and plating or the approach of printing and forming a cream-like pewter on the bump who formed with a photolithography and plating, and the so-called imprint bump method, are learned as an approach of forming a bump in a semi-conductor wafer. Here, the example which produced the golden (Au) bump by the approach by the photolithography and plating explains.
[0024] First, the photograph process of a film resist is performed to the opening 8 which vapor-deposits (drawing 6 (a)) and a barrier metal (Ti, Pd, Cr, Cu) completely to the field of the semi-conductor wafer 11 which has Si3N6 protective coat (drawing 6 (b)), next is formed at a back process (drawing 6 (c)). The opening 8 of a film resist is formed so that a bump B1 may become an elliptical column type. The above-mentioned opening 8 is formed according to the configuration of the bump B1 of the gestalt of each above-mentioned implementation, B-2, B3, and B4. In addition, since each configuration of the bump B1 of the gestalt of each above-mentioned implementation, B-2, B3, and B4 is bilateral symmetry, it can be easily manufactured also in the manufacture process of the bump by the photolithography, plating, etc.
[0025] Then, an acid etc. washes the opening 8 of a film resist, and as shown in drawing 6 (d), golden (Au) plating is formed in the above-mentioned opening 8. And after forming golden (Au) plating in the above-mentioned opening 8, a film resist is removed, barrier metals (Ti, Pd, Cr, Cu, etc.) are formed by etching, and the elliptical column type bump B1 is formed (drawing 6 (e)).
[0026] As mentioned above, the formation approach of the bump of the semiconductor device in the gestalt of this operation can be formed by the conventional general formation approaches, such as an approach by the photolithography and plating, and only the configurations of the opening 8 of a film resist differ.
[0027] (COG mounting) COG mounting of the semiconductor device IC in the gestalt of each above-mentioned implementation is explained. First, as a liquid crystal display is shown in drawing 7 and drawing 8 , the semiconductor device DrIC is mounted in the mounting field 25 of the periphery section of liquid crystal panel LCD. Liquid crystal panel LCD is the reflective mold LCD using TFT which is the typical active component by which current use is carried out. In addition, the semiconductor device IC which makes a liquid crystal panel drive is called the driver DrIC for a drive (Driver IC, Driver LSI).
[0028] If the 1st substrate (one substrate: AM substrate) 1 of liquid crystal panel LCD is larger than the substrate 13 of another side and both the substrates 1 and 13 are piled up for this reason, the mounting field 25 of the semiconductor device DrIC jutted out around the AM substrate 1 in part is formed. The circuit pattern 20 for semi-conductor mounting is formed in the mounting field 25 of this 1st substrate 1. In addition, as an AM substrate 1, the flexible substrate of the product made of synthetic resin besides a glass substrate may be used.
[0029] The semiconductor device of the gestalt of this operation is mounted in the mounting field 25 of a semiconductor device DrIC through the adhesives 26 which have conductivity, as shown in drawing 9 . Along the periphery side, the 1st and the bump B1 of the gestalt of the 2nd operation, and B-2 counter, and a large number formation is carried out at the rear-face side of a semiconductor device DrIC. Gold (Au) is used and, as for bump B-2 which is the electrode of the letter of a projection of this semiconductor device DrIC, the bump array is the same as the gestalt (what is shown in drawing 1 thru/or drawing 5) of the 4th operation from the gestalt of the 1st operation.
[0030] Pattern formation of the electrodes 21 and 22 linked to a semiconductor device DrIC is carried

out around the circuit pattern 20 (both sides in drawing). An electrode 21 (******) is an input electrode and an electrode 22 (******) is an output electrode. And the semiconductor device DrIC which makes liquid crystal panel LCD drive is mounted through the adhesives 26 which have conductivity.

[0031] Although the adhesives 26 which have conductivity are the anisotropy electric conduction film (Anisotropic Conductive Film:ACF) 26, they may be electroconductive glue (conductive paste). Conductive particle 26a is distributed in the adhesives which have insulation, and the anisotropy electric conduction film (Anisotropic Conductive Film:ACF) 26 has conductivity in the thickness direction (the connection direction), has insulation in the direction of a field (longitudinal direction), and consists of conductive particle 26a and adhesives. The connection is heating sticking by pressure fundamentally, and conductive particle 26a takes charge of the function of electrical connection, and it takes charge of the function in which adhesives hold a pressure-welding condition.

[0032] In the connection direction, it is destroyed by the sticking-by-pressure force, the anisotropy electric conduction film 26 carries out the coat of the insulating pellicular resin to the front face of conductive particle 26a, lower layer metal thin film and electrode contact, insulating pellicular resin flows while having a role of a protection sheet of the anisotropy electric conduction film 26, and insulation is maintained, even if it is not destroyed in a longitudinal direction but conductive particle 26a contacts. That is, after the anisotropy electric conduction film 26 is supplied with a configuration like a double-sided tape and sticks an adhesives layer side on a liquid crystal panel before a liquid crystal panel sticks it, it removes a separator, exposes an adhesives layer, mounts a semiconductor device DrIC after that (heating pressurization), stiffens the adhesives of the semiconductor device DrIC section, and obtains original adhesive strength. As insulating pellicular resin, Teflon (trademark) and PET (poly-ethylene terephtalate resin) are used. As adhesives, reliable thermosetting resin is also used besides thermoplastics. In addition, some which plated the metal thin film are shown in the front face of a macromolecule ball at conductive particle 26a.

[0033] A circuit pattern 20 is a wiring group (bus wiring) which performs supply and current supply of the signal to a semiconductor device DrIC (drive driver), and pattern formation is possible for it to coincidence at a component process in the AM substrate 1 (AM-LCD). After the circuit pattern 20 of the gestalt of this operation forms the charge of aluminum lumber to 0.1-0.2 micrometers of thickness by sputtering, by the photolithography, pattern NINGU of it is carried out and it is formed. Since the area rate of an input-electrode 21 and output-electrode 22 top of conductive particle 26a has moreover increased by the thickness whose anisotropy electric conduction film 26 is about 0.2 micrometers, it does not function as adhesives but is functioning as electric conduction film. In addition, the pad part of the edge of a circuit pattern 20 may be made into the same configuration as the configuration of the bump B1 of the gestalt of this operation, B-2, B3, and B4.

[0034] Therefore, in mounting a semiconductor device DrIC in the AM substrate 1 which is a substrate for semi-conductor mounting, as shown in drawing 9 R> 9 (a), it continues throughout the mounting field 25 of the 1st substrate (AM substrate) 1, and supplies the anisotropy electric conduction film 26.

[0035] Next, it mounts by having supplied the anisotropy electric conduction film 26 upwards, and carrying out thermocompression bonding of the semiconductor device IC in which alignment was carried out with the wearing machine, and the golden bump B1 (B-2, B3, and B4 are included) was formed (drawing 9 (b)). In this case, the former, There was a case where conductive particle 26a of the anisotropy electric conduction film (ACF) 26 inclines, and spread around a bump B1 (B-2, B3, and B4 are included), or air comes to be pushed in and air bubbles K were made (refer to drawing 12). However, with the gestalt of this operation, since the golden bump B1 formed in the semiconductor device IC is an elliptical column type etc., generating of breadth (refer to the arrow head in drawing 1 and drawing 2) and the air bubbles K by the fluidity of the anisotropy electric conduction film (ACF) 26 being checked like before is not produced so that the anisotropy electric conduction film (ACF) 26 may flow smoothly in the direction of a periphery of a semiconductor device IC. Therefore, the conductive particle of the partial anisotropy electric conduction film (ACF) short-circuits horizontally, or a possibility of making a semiconductor device and a substrate producing a crack by the difference in the coefficient of thermal expansion of a paste-like ingredient and air does not have it, either. In addition, in the case of column [with which the cross section in the gestalt of the 2nd operation has the narrow streamline shape R1 of bilateral symmetry] type bump B-2, still more smooth flow is secured along with the narrow streamline shape R1. Moreover, although, especially as for COG mounting, the

inclination of a miniaturization and thin-shape-izing of a liquid crystal panel to the mounting field 25 is restricted, the bump B1 of the gestalt of each above-mentioned implementation and B-2 (B3 and B4 are included) can attain fine pitch-ization from the conventional rectangular parallelepiped or the forward circular-like bump B.

[0036] By the way, in COG mounting, since the substrate for semi-conductor mounting was the AM substrate 1 made into one substrate of a liquid crystal panel, and one, when carrying out thermocompression bonding of the semiconductor device DrIC and paste-like ingredient 26 grade did not spread in the direction of a periphery smoothly, it has a possibility of becoming the load stress at the time of carrying out thermocompression bonding of the semiconductor device DrIC, and the yield of a direct liquid crystal panel might be influenced. However, when the anisotropy electric conduction film (ACF) 26 flows smoothly in the direction of a periphery of a semiconductor device DrIC by the semiconductor device DrIC which has the bump B1 of the gestalt of this operation, and B-2 (B3 and B4 are included), load stress is mitigated and mounting which does not influence the yield of a liquid crystal panel is performed.

[0037] (Mounting of the general semiconductor device IC) TAB (tape automatedbonding) which is the mounting method of the semiconductor device which used the adhesives which have conductivity although the mounting structure of the above-mentioned semiconductor device DrIC explained COG mounting to the example -- it is applicable also to law and the mounting approach of the semiconductor device of the general circuit board. As the circuit board of the general circuit board, the flexible substrate of the product made of synthetic resin besides a glass substrate may be used.

[0038] However, in general mounting of a semiconductor device IC, in order to secure the junction force of the semiconductor device IC besides the anisotropy electric conduction film (ACF) 26 or electroconductive glue (conductive paste), and a substrate 31, the resin for the closures may be enclosed. Below, the 3rd and the bump B3 in the gestalt of the 4th operation, and B4 are used. Ingredients, such as anisotropy electric conduction film (ACF) and electroconductive glue (conductive paste), etc. are supplied only on the bump B1 of a semiconductor device IC. After mounting this with heating / pressurization means, the resin 37 for the closures for securing these junction is slushed between a semiconductor device IC and a substrate 31, and how to stiffen this is explained.

[0039] Drawing 10 is mounting process drawing of the semiconductor device IC with a bump, and shows how to mount the semiconductor device IC in which a bump B3 and B4 were formed in the substrate 31 for semi-conductor mounting. The sign 34 shows the circuit pattern on the substrate 3 for semi-conductor mounting.

[0040] A semiconductor device IC is faced mounting in the substrate 31 for semi-conductor mounting. As shown in drawing 10 (a), the ingredient 36 of the shape of the shape of a paste, such as anisotropy electric conduction film (Anisotropic Conductive Film:ACF) and electroconductive glue (conductive paste), and a film is imprinted only on the bump B3 of a semiconductor device IC, and B4. Alignment is carried out with a wearing machine and the semiconductor device IC in which the golden bump B3 was formed is mounted by thermocompression bonding (drawing 10 (b)). Next, the resin 37 for the closures for securing these junction is slushed between a semiconductor device IC and a substrate 31, and this is stiffened.

[0041] Since the golden bump B3 and B4 which were formed in the semiconductor device IC are the column type of the rhombus configuration where that cross section is long and slender when the resin 37 for these closures is slushed, the fluidity of the resin 37 for the closures is not checked like the bump B of the conventional rectangular parallelepiped. Therefore, generating of the air bubbles K by the fluidity of a paste-like ingredient being checked like before is not produced. In addition, in the case of bump B4 in the gestalt of the 4th operation which has the part R2 from which the cross section serves as narrow by the shape of a long and slender polygon of bilateral symmetry, flow still more smooth than the thing of the gestalt of implementation of the above 3rd is secured.

[0042] (MCM mounting) Next, mounting used for the multi chip module (henceforth MCM) which carries out the modularization of two or more semiconductor devices IC, and mounts them is explained.

[0043] As shown in drawing 11 (a) and (b), two or more semiconductor devices IC are mounted in the module substrate 41, respectively. In this case, it is mounted through the adhesives 26 which have the conductivity of the anisotropy electric conduction film (ACF) etc., and MCM is completed. Here, the above-mentioned golden bump B1 and a circuit pattern 45 are joined through the adhesives 26 which

have conductivity. It seems that namely, air bubbles K are not generated when a paste-like ingredient etc. flows smoothly in the direction of a periphery of a semiconductor device IC even if it faces MCM mounting of the gestalt of this operation. Then, MCM is joined to the mother substrate 43 with other electronic devices 42. In this case, a bump is formed with a pewter, it considers as the so-called pewter bump 44, melting solidification of the pewter bump 44 is carried out by the reflow, and it connects with the electrode of a substrate (it corresponds to the 1st conventional approach). In addition, in case it joins to the mother substrate 43, you may join using the adhesives 26 which have conductivity.

[0044]

[Effect of the Invention] Since it has the configuration and directivity from which a bump becomes narrow toward the direction of a periphery of a semiconductor device, the semiconductor device concerning this invention will spread in homogeneity so that a paste-like ingredient etc. may flow smoothly in the direction of a periphery of a semiconductor device. Therefore, it becomes possible to generate air bubbles, not to produce the situation [like] and to attain a bump's fine pitch-ization moreover.

[0045] Since it has the configuration from which a bump becomes narrow toward the direction of a periphery of a semiconductor device, the liquid crystal display with which the semiconductor device concerning this invention was mounted will spread in homogeneity so that a paste-like ingredient etc. may flow smoothly in the direction of a periphery of a semiconductor device. Therefore, also in COG mounting, the load which is not made to produce the situation which generates air bubbles and is moreover applied to one substrate of a liquid crystal panel is mitigated, and it becomes possible to offer the liquid crystal display with which the semiconductor device with high junction dependability was mounted. Moreover, it becomes possible to attain a bump's fine pitch-ization in COG mounting as which a miniaturization and thin shape-ization are required.

[0046]

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the perspective view in which drawing showing the semiconductor device of the gestalt of operation of the 1st of this invention and (a) show the top view, and (b) shows the bump.
[Drawing 2] It is the perspective view in which drawing showing the semiconductor device of the gestalt of operation of the 2nd of this invention and (a) show the top view, and (b) shows the bump.
[Drawing 3] It is the perspective view in which drawing showing the semiconductor device of the gestalt of operation of the 3rd of this invention and (a) show the top view, and (b) shows the bump.
[Drawing 4] It is the perspective view in which drawing showing the semiconductor device of the gestalt of operation of the 4th of this invention and (a) show the top view, and (b) shows the bump.
[Drawing 5] The perspective view showing the bump of the application of the gestalt of each above-mentioned implementation
[Drawing 6] Drawing explaining the formation process of the bump of the gestalt of each above-mentioned implementation
[Drawing 7] The perspective view showing the mounting structure of the semiconductor device of the liquid crystal display of this invention
[Drawing 8] The sectional view showing the liquid crystal display of the gestalt of top Norikazu operation
[Drawing 9] The sectional view showing the process of COG mounting
[Drawing 10] The sectional view showing the mounting process of a general semiconductor device
[Drawing 11] For drawing showing the example of MCM mounting, and (a), the top view and (b) are the sectional view.
[Drawing 12] Drawing showing the example of the conventional semiconductor device
[Drawing 13] Drawing showing the example of the conventional semiconductor device
[Description of Notations]
1, 31, 41, 43 Substrate for semi-conductor mounting,
8 [ ] Opening of Film Resist,
11 [ ] Semi-conductor Wafer,
20 34 Circuit pattern
25 [ ] Mounting Field,
26 36 Adhesives which have conductivity (paste-like ingredient),
26a [ ] a conductive particle,
37 [ ] Resin for Closures,
B, B1, B-2, B3, B4 Bump,
IC, DrIC Semiconductor device,
R1 Narrow streamline shape,
R2 Part which serves as narrow by the shape of a long and slender polygon

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[Translation done.]

* NOTICES *

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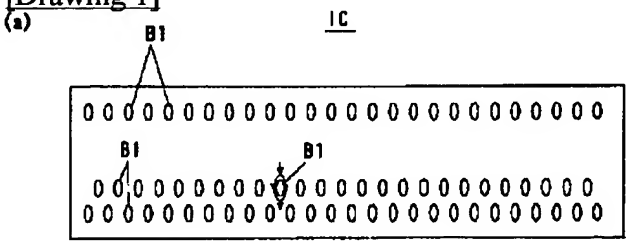
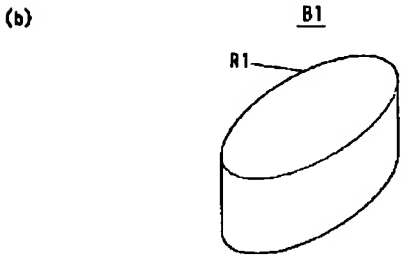
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]





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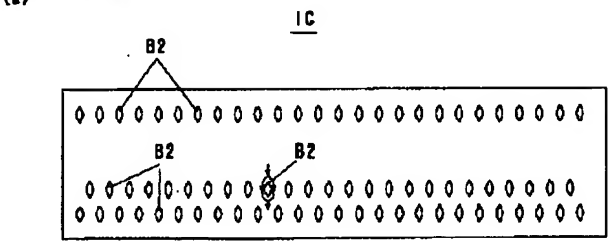

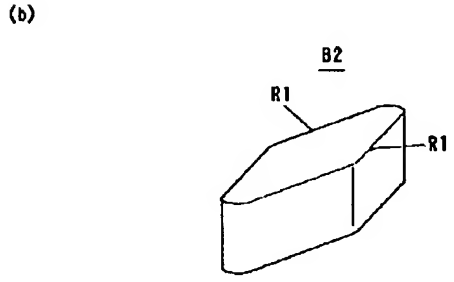

[Drawing 3]

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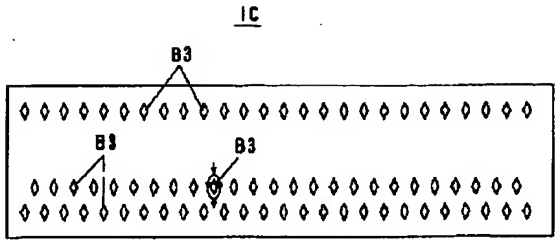

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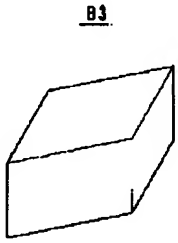

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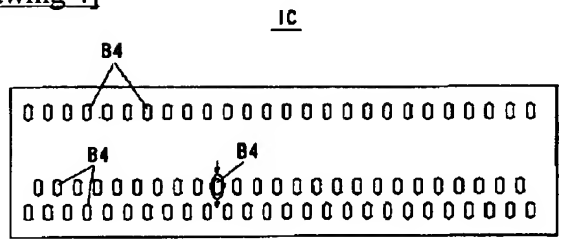

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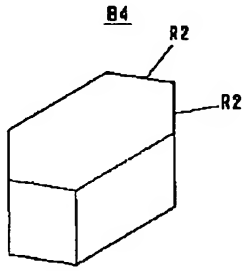

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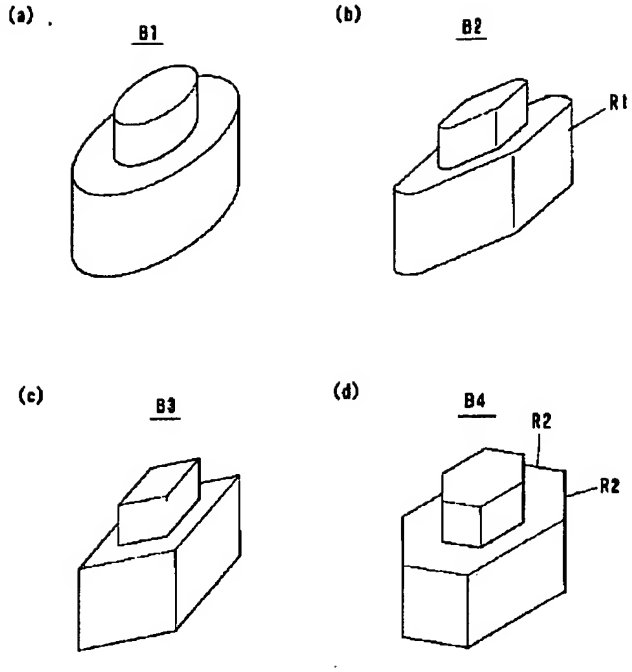

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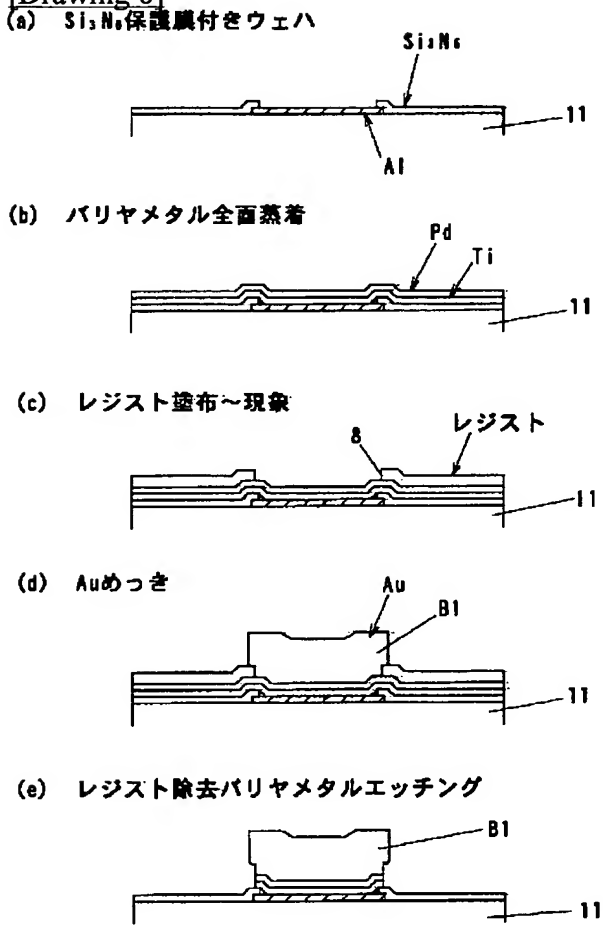

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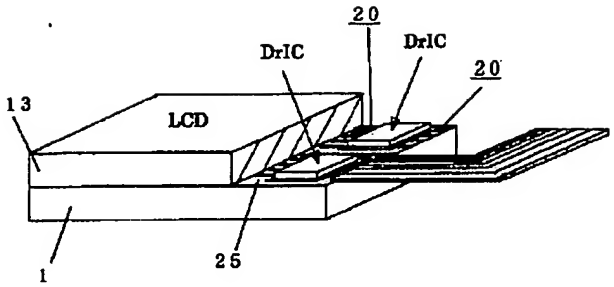

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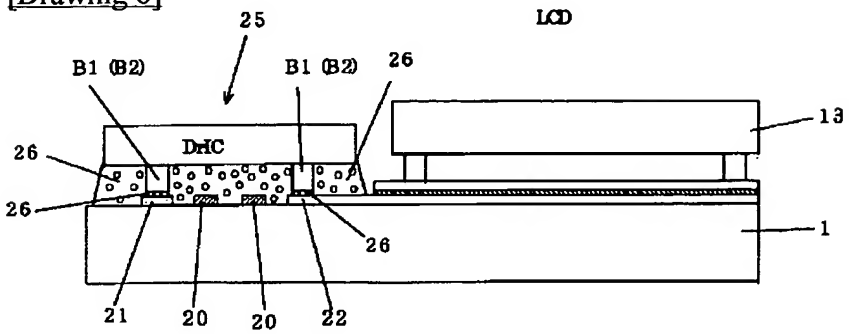

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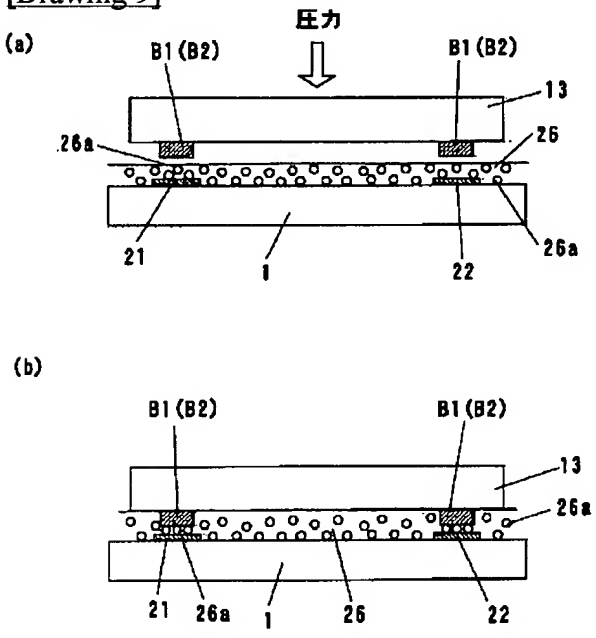

[Drawing 10]

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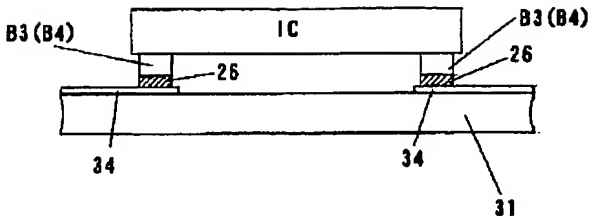

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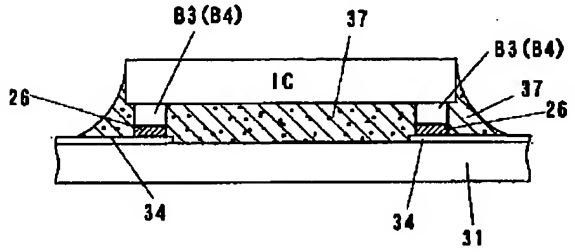

[Drawing 11]

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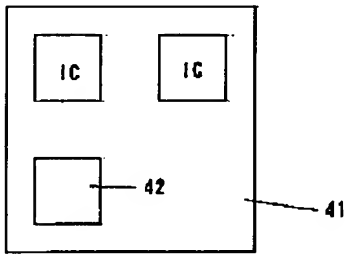

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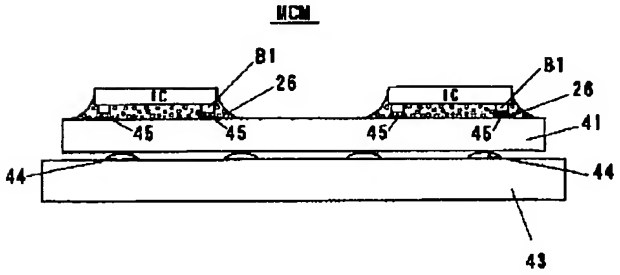

[Drawing 12]

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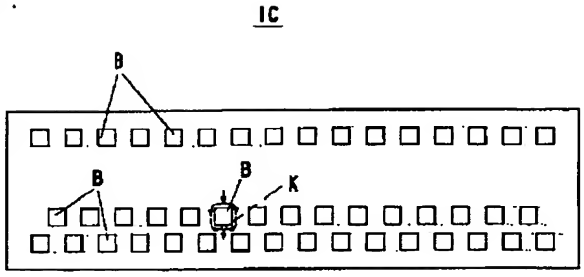

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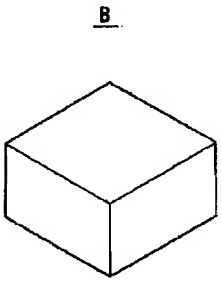

[Drawing 13]

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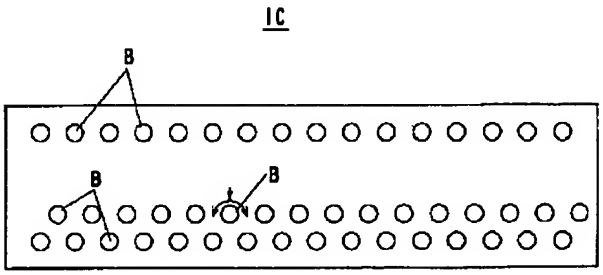

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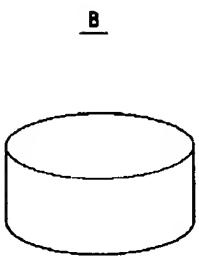

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Drawing selection Representative drawing

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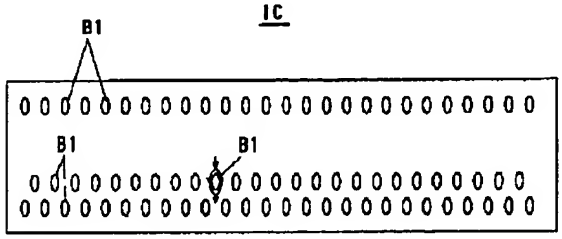

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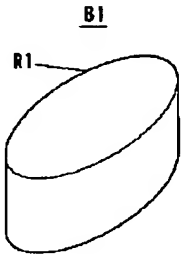

[Translation done.]

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] For the above-mentioned bump, the cross section is the semiconductor device which the cross section is the column type with which it has an elliptical column type or the narrow streamline shape of bilateral symmetry in the semiconductor device which has the bump mounted in the substrate for semi-conductor mounting through the ingredient of the shape of the shape of a paste, and a film, and is characterized by arranging the part used as narrow [these] toward the direction of a periphery of a semiconductor device.
[Claim 2] It is the semiconductor device which is the column type which has the part from which the above-mentioned bump becomes narrow in the semiconductor device which has the bump mount in the substrate for semi-conductor mounting through the ingredient of the shape of the shape of a paste , and a film by the shape of a polygon with the column type of the rhombus configuration where of the cross section is long and slender or its cross section long and slender , in the direction of axial symmetry and its symmetry line , and is characterize by to be arrange the part used as narrow [these] toward the direction of a semiconductor device of a periphery .
[Claim 3] Said bump is a semiconductor device according to claim 1 or 2 characterized by shifting a mutual train and being alternately arranged while consisting of two or more trains along the periphery edge of a semiconductor device.
[Claim 4] It is the liquid crystal display with which the semiconductor device according to claim 1 to 3 which the ingredients of the shape of said shape of a paste and a film are the adhesives which have conductivity, and is characterized by the substrates for said semi-conductor mounting being one substrate of the liquid crystal panel by which liquid crystal was ****(ed) between the substrates which counter, and a substrate made into one was mounted.

[Translation done.]

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Ｇ０２Ｆ　1/1345		Ｈ０１Ｌ　21/60	３１１Ｓ	５Ｆ０４４
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			６０２Ｎ	

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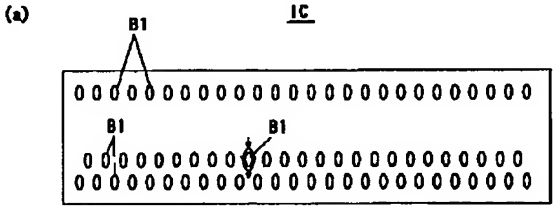
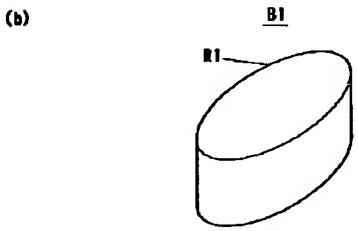
Ｆターム(参考)　2H092 GA48 GA50 GA60 NA11 NA29 PA06
5F044 KK06 LL07 QQ02

(54)【発明の名称】　半導体素子及びその半導体素子が実装された液晶表示装置

(57)【要約】
【課題】　ペースト状材料等のスムーズな流れを確保するとともに、バンプのファインピッチ化を図る。
【解決手段】　半導体実装用の基板にペースト状材料若しくはフィルム状の材料を介して実装されるバンプＢ１を有する半導体素子ＩＣにおいて、上記バンプＢ１は、その断面が楕円形状の柱型であり、この幅狭となる部分が半導体素子ＩＣの外周方向に向かって配置されている。





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【特許請求の範囲】

【請求項1】　半導体実装用の基板にペースト状若しくはフィルム状の材料を介して実装されるバンプを有する半導体素子において、

上記バンプは、その断面が楕円形状の柱型、又は、その断面が左右対称の幅狭の流線形を有する柱型であり、これらの幅狭となる部分が半導体素子の外周方向に向かって配置されていることを特徴とする半導体素子。

【請求項2】　半導体実装用の基板にペースト状若しくはフィルム状の材料を介して実装されるバンプを有する半導体素子において、

上記バンプは、その断面が細長い菱形形状の柱型、又は、その断面が線対称かつその対称線の方向に細長い多角形状で幅狭となる部分を有する柱型であり、これらの幅狭となる部分が半導体素子の外周方向に向かって配置されていることを特徴とする半導体素子。

【請求項3】　前記バンプは、半導体素子の外周縁に沿って複数列で構成されるとともに互いの列をずらして千鳥状に配列されていることを特徴とする請求項1又は請求項2記載の半導体素子。

【請求項4】　前記ペースト状若しくはフィルム状の材料が導電性を有する接着剤であり、

前記半導体実装用の基板は、対向する基板間に液晶が狭持された液晶パネルの一方の基板と一体とされた基板であることを特徴とする請求項1乃至請求項3記載の半導体素子が実装された液晶表示装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、ＩＣチップやＬＳＩチップなどの半導体素子及びその半導体素子が実装された液晶表示装置に関する。

【0002】

【従来の技術】ＩＣチップやＬＳＩチップなどの半導体素子として、突起状の電極であるバンプを有するものが半導体実装用の基板の小型化やモジュールの薄型化などに有利なことから、各種コンピュータや液晶表示装置などの電子機器に多く用いられている。この突起状の電極であるバンプは、その材質として、ハンダや、金（Ａｕ）、銀（Ａｇ）、銅（Ｃｕ）、鉛（Ｐｄ）、ニッケル（Ｎｉ）などが利用され、フォトリソグラフィとメッキ法による方法、或いは、フォトリソグラフィとメッキ法によって形成したバンプ上にクリーム状ハンダを印刷して形成する方法、いわゆる転写バンプ法等の多くの方法が従来から存在する。

【0003】このようなバンプ付き半導体素子を基板にフェースダウンで実装する方法としては、従来から様々な方法が提案されている。代表的な方法は次の通りである。まず第1に、バンプをハンダにより球形状や半球状に形成して、いわゆるハンダバンプとし、リフローによりハンダバンプを溶融固化させて基板の電極に接続する

2

方法がある。なお、バンプを金により形成した金バンプとし、また基板の電極上にメッキ等によりハンダをプリコートし、上記方法と同様にリフローによりハンダ付けし、好ましくは、半導体素子と基板の接合力を確保するために封止用の樹脂が封入される方法もある。

【0004】次に第2に、半導体素子を実装するに際して、基板上の装着領域の全体に亘ってペースト状材料若しくはフィルム状の材料を供給し、その上から半導体素子を装着機で位置決めをして、加熱及び加圧手段によりペースト状材料等を硬化させる方法がある。ペースト状材料若しくはフィルム状の材料としては、異方性導電膜（Anisotropic Conductive Film：ACF）や熱圧着絶縁硬化樹脂などがある。

【0005】次に第3に、半導体素子を実装するに際して、半導体素子のバンプ上にのみ異方性導電膜（Anisotropic Conductive Film：ACF）や導電性接着剤（導電性ペースト）等の材料を転写し、これを加熱手段で硬化させた後、半導体素子と基板の間にこれらの接合を確保するための封止用の樹脂を流し込み、これを硬化させる方法がある。第2の方法と第3の方法のバンプとしては、断面が四角形状の柱型（直方体）や正円形状の柱型（円柱型）の金であることが通常であるが、この金バンプ先端にハンダバンプが球形状や半球状に形成されて使用されることもある（多層構造のバンプ）。

【0006】

【発明が解決しようとする課題】ところで、近年の半導体素子の高密度化と半導体実装用の基板の更なる小型化に伴って、バンプ配列はピッチが狭くなる傾向にある（バンプのファインピッチ化）。そして、図12及び図13に示すように、バンプBの配列をいわゆる千鳥構成の複数配列としたバンプBの更なるファインピッチ化が進んでいる。

【0007】一方、液晶表示装置における半導体素子の実装では、ガラス基板上の電極端子に直接半導体素子を接続するＣＯＧ（chip on glass）実装がある。ガラス基板の代わりにプラスチック製のフレキシブル基板が用いられることもあるが（これをＣＯＦ（chip on flexible）、ＣＯＰ（chip on plastic）と呼ぶこともある。）、これらＣＯＧ実装等は、液晶パネルの小型化・薄型化が著しい液晶表示装置の分野において今後主流となるものと予想されている。ＣＯＧ実装では、異方性導電膜と導電性接着剤が併存して使用され、上記形状の金バンプBを有する半導体素子ＩＣの実装が通常である。

【0008】しかしながら、半導体素子ＩＣを半導体実装用の基板に実装するに際して、異方性導電膜、導電性接着剤や半導体素子と基板を封止する封止用樹脂等のペースト状若しくはフィルム状の材料を介在させて実装するが、上記バンプBの形状により、ペースト状材料等が半導体素子ＩＣの外周方向（下流方向）にスムーズに広がらない事態、すなわち、流動性を阻害する事態が生じ

る問題を有する。

【0009】具体的には、図12に示すように、その断面が四角形状の柱型（直方体）であるバンプBの半導体素子ICの場合は、バンプBの周辺にペースト状若しくはフィルム状材料及び異方性導電膜（ACF）の導電性粒子が偏って行き渡ったり、空気が押し込められるようになって気泡Kができたりする場合がある。この気泡Kができた状態で冷却すると、ペースト状材料と空気の熱膨張係数の違いにより半導体素子や基板に亀裂を生じさせたり、特に異方性導電膜（ACF）を用いた場合は、気泡Kの回りに導電性粒子が凝集し、水平方向にショートさせる等の問題を誘発したりする。また、バンプBが正円形の柱型（円柱型）である場合は、図13に示すように、ペースト状材料等の広がりがバンプ列に平行となる方向に偏り、実装領域に均等に広がらない事態（流動性を阻害する事態）を生じさせていた。これらの問題は、特にバンプBのピッチが狭い場合や複数列で構成されている場合は、その傾向が顕著でその問題は大きなものとなる。

【0010】また、COG実装では、上記問題の他に、半導体実装用の基板が液晶パネルの一方の基板と一体とされているので、ペースト状材料等がスムーズに外周方向に広がらないと、半導体素子を熱圧着する際の荷重ストレスとなるおそれを有し、直接液晶パネルの歩留まりに影響することもあった。

【0011】そして、バンプのファインピッチ化が要求される今日、直方体や円柱型のものでは、接続信頼性に優れるとともに製造プロセスにおいて製造し易いというような利点はあるものの、バンプのファインピッチ化には限界が生じていた。

【0012】そこで、本発明の目的は、半導体素子を半導体実装用の基板に実装するに際して、気泡を発生させないペースト状材料等のスムーズな流れの均一な広がりを確保するとともに、バンプのファインピッチ化を図ることが可能な半導体素子及びその半導体素子が実装された液晶表示装置を提供することにある。

【0013】

【課題を解決するための手段】本発明の請求項1記載の半導体素子は、半導体実装用の基板にペースト状若しくはフィルム状の材料を介して実装されるバンプを有する半導体素子において、上記バンプは、その断面が楕円形状の柱型、又は、その断面が左右対称の幅狭の流線形を有する柱型であり、これらの幅狭となる部分が半導体素子の外周方向に向かって配置されていることを特徴とする。

【0014】本発明の請求項2記載の半導体素子は、半導体実装用の基板にペースト状若しくはフィルム状の材料を介して実装されるバンプを有する半導体素子において、上記バンプは、その断面が細長い菱形形状の柱型、又は、その断面が線対称かつその対称線の方向に細長い多角形状で幅狭となる部分を有する柱型であり、これらの幅狭となる部分が半導体素子の外周方向に向かって配置されていることを特徴とする。

【0015】これら請求項1又は請求項2記載の発明によれば、半導体実装用の基板にペースト状材料等を介して半導体素子を実装する際に、ペースト状材料等が半導体素子の外周方向に流れるように均一に広がるが、上記形状と方向性を有するバンプは半導体素子の外周方向に向かって幅狭となるために、ペースト状材料等が半導体素子の外周方向にスムーズに流れるように均一に広がり、ペースト状材料及び異方性導電膜（ACF）の導電性粒子が偏ったり、ペースト状材料等の流動性が阻害されることによる気泡が発生したりするようなことがなくなる。また、幅狭となる部分が半導体素子の外周方向に向かって配置されていることから、従来の断面が四角形状の柱型（直方体）や正円形状の柱型（円柱状）のものと比較してバンプのファインピッチ化を図ることができる。なお、バンプの断面形状はいずれも線対称であるから、従来フォトリソグラフィとメッキ法等によるバンプの製造プロセスにおいても容易に製造可能である。

【0016】本発明の請求項3記載の半導体素子は、前記バンプは、半導体素子の外周縁に沿って複数列で構成されるとともに互いの列をずらして千鳥状に配列されていることを特徴とする。

【0017】この発明によれば、バンプが互いの列をずらして千鳥状に複数配列されている場合でも、ペースト状材料等が流れるように均一に広がることとなり、バンプのファインピッチ化の要請に対応することとなる。

【0018】本発明の請求項4記載の半導体素子が実装された液晶表示装置は、前記ペースト状若しくはフィルム状の材料が導電性を有する接着剤であり、前記半導体実装用の基板は、対向する基板間に液晶が狭持された液晶パネルの一方の基板と一体とされた基板であることを特徴とする。

【0019】この発明によれば、ペースト状若しくはフィルム状材料である異方性導電膜（ACF）が半導体素子の外周方向にスムーズに流れるように均一に広がり、異方性導電膜（ACF）の導電性粒子が偏ったり、異方性導電膜（ACF）の流動性が阻害されることにより気泡が発生したりするようなことがなくなる。また、液晶パネルの一方の基板と一体とされた半導体実装用の基板においても、半導体素子を熱圧着する際に基板に荷重ストレスがかかるおそれもなくなる。

【0020】

【発明の実施の形態】以下、本発明の実施の形態を、図面を引用しながら説明する。なお、本発明のバンプを有する半導体素子の実施の形態、バンプの製造プロセス、バンプを有する半導体素子のCOG実装、一般の半導体素子ICの実装、MCM実装の順に説明する。

【0021】半導体素子ICには、複数のバンプB1が

形成されている。バンプB1は、金（Au）が使用され、図1に示すように、一方の側のバンプ配列は、半導体素子ICの外周縁に沿って一列で構成され、他方側のバンプ配列は、半導体素子ICの外周縁に沿って複数列で構成されるとともに、互いの列をずらして千鳥状に配列されている。各バンプB1の形状は、その断面が楕円形状の柱型である（第1の実施の形態）。すなわち、半導体素子ICの外周方向に向かって左右対称に幅狭となる柱型である。このようなバンプB1の例としては、上記楕円形状と同様、その断面が線対称の幅狭の流線形R1を有するものであれば、図2に示すように、水滴状のような柱型のバンプB2でも良い（第2の実施の形態）。さらに、図5（a）（b）に示す応用例のように、このようなバンプB1，B2は、その形状が相似形の多層構造であっても良い。そして、何れも異方性導電膜（ACF）等のペースト状若しくはフィルム状材料を半導体素子ICの外周方向にスムーズに押し流すために、幅狭となる部分が半導体素子ICの外周方向に向かって配置されている。

【0022】また、バンプB3の形状は、図3に示すように、その断面が細長い菱形形状の柱型でも良い（第3の実施の形態）。また、上記細長い菱形形状と同様、その断面が線対称かつその対称線の方向に細長い多角形状で幅狭となる部分R2を有する柱型であれば、図4に示すように、細長い六角形状や、その他の細長い多角形状であっても良い（第4の実施の形態）。さらに、図5（b）（c）に示す応用例のように、このようなバンプB3，B4としては、その形状が相似形の多層構造であっても良い。

【0023】（バンプの形成プロセス）次に、上記各実施の形態のバンプB1，B2，B3，B4の形成プロセスを説明する。一般的に、半導体ウェハにバンプを形成する方法として、フォトリソグラフィとメッキ法による方法、或いは、フォトリソグラフィとメッキ法によって形成したバンプ上にクリーム状ハンダを印刷して形成する方法、いわゆる転写バンプ法等の多くの方法が知られている。ここではフォトリソグラフィとメッキ法による方法で金（Au）バンプを作製した例で説明する。

【0024】まず、Si_3N_6保護膜を有する半導体ウェハ11の面に（図6（a））、バリヤメタル（Ti，Pd，Cr，Cu）を全面蒸着して（図6（b））、次に、後工程で形成される開口部8にフィルムレジストのフォト工程を行う（図6（c））。フィルムレジストの開口部8は、バンプB1が楕円形状の柱型になるように形成されている。上記開口部8は、上記各実施の形態のバンプB1，B2，B3，B4の形状に合わせて形成する。なお、上記各実施の形態のバンプB1，B2，B3，B4の形状はいずれも左右対称であるから、フォトリソグラフィとメッキ法等によるバンプの製造プロセスにおいても容易に製造可能である。

【0025】その後、酸などによりフィルムレジストの開口部8を洗浄し、図6（d）に示すように、上記開口部8に金（Au）メッキを形成する。そして、上記開口部8に金（Au）メッキを形成した後、フィルムレジストを除去し、バリヤメタル（Ti，Pd，Cr，Cu等）をエッチングにより形成して、楕円形状の柱型のバンプB1を形成する（図6（e））。

【0026】以上のように、本実施の形態における半導体素子のバンプの形成方法は、フォトリソグラフィとメッキ法による方法等の従来の一般的な形成方法で形成可能であり、フィルムレジストの開口部8の形状のみが異なる。

【0027】（COG実装）上記各実施の形態における半導体素子ICのCOG実装について説明する。まず、液晶表示装置は、図7及び図8に示すように、液晶パネルLCDの周縁部の実装領域25に半導体素子DrICが実装されている。液晶パネルLCDは、現在使用されている代表的なアクティブ素子であるTFTを用いた反射型LCDである。なお、液晶パネルを駆動させる半導体素子ICは、駆動用ドライバ（Driver IC、Driver LSI）DrICと呼ばれる。

【0028】液晶パネルLCDの第1の基板（一方の基板：AM基板）1は、他方の基板13よりも大きく、このため両基板1，13を重ね合わせると、AM基板1の周辺に一部張り出した半導体素子DrICの実装領域25が形成されている。この第1の基板1の実装領域25には、半導体実装用の配線パターン20が形成されている。なお、AM基板1としてはガラス基板の他、合成樹脂製のフレキシブル基板でも良い。

【0029】本実施の形態の半導体素子は、図9に示すように、半導体素子DrICの実装領域25に、導電性を有する接着剤26を介して実装されている。半導体素子DrICの裏面側には、外周辺に沿って第1及び第2の実施の形態のバンプB1，B2が対向して多数形成されている。この半導体素子DrICの突起状の電極であるバンプB2は、金（Au）が使用され、バンプ配列は、第1の実施の形態から第4の実施の形態（図1乃至図5に示すもの）と同一である。

【0030】配線パターン20の周辺（図中両側）には、半導体素子DrICに接続する電極21，22がパターン形成されている。電極21（図中左）は、入力電極であり、電極22（図中左）は、出力電極である。そして、導電性を有する接着剤26を介して、液晶パネルLCDを駆動させる半導体素子DrICが実装されている。

【0031】導電性を有する接着剤26は、異方性導電膜（Anisotropic Conductive Film：ACF）26であるが、導電性接着剤（導電性ペースト）であっても良い。異方性導電膜（Anisotropic Conductive Film：ACF）26は、絶縁性を有する接着剤中に導電性粒子26aが分

散され厚み方向（接続方向）に導電性を有し、面方向（横方向）に絶縁性を有するもので、導電性粒子２６ａと接着剤から構成される。その接続は基本的には加熱圧着であり、導電性粒子２６ａが電気接続の機能を担当し、接着剤が圧接状態を保持する機能を担当する。

【００３２】異方性導電膜２６は、導電性粒子２６ａの表面に絶縁性薄膜樹脂をコートするもので、絶縁性薄膜樹脂は、異方性導電膜２６の保護シートとしての役割を有するとともに、接続方向では圧着力で破壊され下層の金属薄膜と電極が接触して導通し、横方向では破壊されず導電性粒子２６ａ同士が接触しても絶縁性が保たれるようになっている。すなわち、異方性導電膜２６は、液晶パネルの貼り付ける前は両面テープのような構成で供給され、液晶パネルに接着剤層側を貼り付けた後、セパレータを剥がし接着剤層を露出させ、その後、半導体素子ＤｒＩＣを実装（加熱加圧）し、半導体素子ＤｒＩＣ部の接着剤を硬化させ、本来の接着力を得る。絶縁性薄膜樹脂としては、テフロン（登録商標）やＰＥＴ（poly-ethylene terephtalate resin）が使用されている。接着剤としては、熱可塑性樹脂の他に信頼性の高い熱硬化性樹脂も使用されている。なお、導電性粒子２６ａには、高分子球の表面に金属薄膜をメッキしたものもある。

【００３３】配線パターン２０は、半導体素子ＤｒＩＣ（駆動ドライバ）への信号の供給や電源供給を行う配線群（バス配線）であり、ＡＭ基板１（ＡＭ－ＬＣＤ）では、素子工程で同時にパターン形成が可能なものである。本実施の形態の配線パターン２０は、アルミニウム製材料をスパッタリングで膜厚０．１～０．２μｍに成膜した後、フォトリソグラフィでパターンニングして形成されている。入力電極２１と出力電極２２上は、異方性導電膜２６が０．２μｍ程度の厚みでしかも導電性粒子２６ａの面積割合が多くなっているため、接着剤として機能しておらず、導電膜として機能している。なお、配線パターン２０の端部のパッド部分を本実施の形態のバンプＢ１，Ｂ２，Ｂ３，Ｂ４の形状と同一形状にしても良い。

【００３４】したがって、半導体素子ＤｒＩＣを半導体実装用の基板であるＡＭ基板１に実装する場合には、図９（ａ）に示すように、第１の基板（ＡＭ基板）１の実装領域２５の全域に亘って異方性導電膜２６を供給する。

【００３５】次に、異方性導電膜２６を供給した上に、装着機で位置合わせし、金バンプＢ１（Ｂ２，Ｂ３，Ｂ４を含む）の形成された半導体素子ＩＣを熱圧着させて実装する（図９（ｂ））。この場合、従来は、バンプＢ１（Ｂ２，Ｂ３，Ｂ４を含む）の周辺に異方性導電膜（ＡＣＦ）２６の導電性粒子２６ａが偏って行き渡ったり、空気が押し込められるようになって気泡Ｋができたりする場合があった（図１２参照）。しかし、本実施の形態では、半導体素子ＩＣに形成された金バンプＢ１が楕円形状の柱型等であるために、異方性導電膜（ＡＣＦ）２６が半導体素子ＩＣの外周方向にスムーズに流れるように広がり（図１、図２中の矢印参照）、従来のように異方性導電膜（ＡＣＦ）２６の流動性が阻害されることによる気泡Ｋの発生を生じさせることがない。したがって、偏った異方性導電膜（ＡＣＦ）の導電性粒子が水平方向にショートしたり、ペースト状材料と空気の熱膨張係数の違いにより半導体素子や基板に亀裂を生じさせたりするおそれもない。なお、第２の実施の形態におけるその断面が左右対称の幅狭の流線形Ｒ１を有する柱型のバンプＢ２の場合は、その幅狭の流線形Ｒ１に沿って更にスムーズな流れが確保される。また、ＣＯＧ実装は、液晶パネルの小型化・薄型化の傾向から実装領域２５が特に制限されるが、上記各実施の形態のバンプＢ１，Ｂ２（Ｂ３，Ｂ４を含む）は、従来の直方体や正円形状のバンプＢよりもファインピッチ化を図ることができる。

【００３６】ところで、ＣＯＧ実装では、半導体実装用の基板が液晶パネルの一方の基板と一体とされているＡＭ基板１であるために、半導体素子ＤｒＩＣを熱圧着する際に、ペースト状材料２６等がスムーズに外周方向に広がらないと、半導体素子ＤｒＩＣを熱圧着する際の荷重ストレスとなるおそれを有し、直接液晶パネルの歩留まりに影響することもあった。しかしながら、本実施の形態のバンプＢ１，Ｂ２（Ｂ３，Ｂ４を含む）を有する半導体素子ＤｒＩＣにより、異方性導電膜（ＡＣＦ）２６が半導体素子ＤｒＩＣの外周方向にスムーズに流れることにより、荷重ストレスが軽減され、液晶パネルの歩留まりに影響しない実装が行われる。

【００３７】（一般の半導体素子ＩＣの実装）上記半導体素子ＤｒＩＣの実装構造は、ＣＯＧ実装を例に説明したが、導電性を有する接着剤を使用した半導体素子の実装方式であるＴＡＢ（tape automatedbonding）法や、回路基板一般への半導体素子の実装方法にも適用可能である。回路基板一般の回路基板としては、ガラス基板の他、合成樹脂製のフレキシブル基板でも良い。

【００３８】ただし、一般的な半導体素子ＩＣの実装の場合、異方性導電膜（ＡＣＦ）２６や導電性接着剤（導電性ペースト）の他、半導体素子ＩＣと基板３１の接合力を確保するために封止用の樹脂が封入される場合がある。以下では、第３及び第４の実施の形態におけるバンプＢ３，Ｂ４を使用して、半導体素子ＩＣのバンプＢ１上にのみ異方性導電膜（ＡＣＦ）や導電性接着剤（導電性ペースト）等の材料等を供給し、これを加熱・加圧手段で実装した後、半導体素子ＩＣと基板３１の間にこれらの接合を確保するための封止用の樹脂３７を流し込み、これを硬化させる方法について説明する。

【００３９】図１０は、バンプ付き半導体素子ＩＣの実装工程図であって、バンプＢ３，Ｂ４の形成された半導

体素子ＩＣを半導体実装用の基板３１に実装する方法を示している。符号３４は半導体実装用の基板３上の配線パターンを示している。

【００４０】半導体素子ＩＣを半導体実装用の基板３１に実装するに際しては、図１０（ａ）に示すように、半導体素子ＩＣのバンプＢ３，Ｂ４上にのみ異方性導電膜（Anisotropic Conductive Film：ACF）や導電性接着剤（導電性ペースト）等のペースト状若しくはフィルム状の材料３６を転写し、装着機で位置合わせし、金バンプＢ３の形成された半導体素子ＩＣを熱圧着により実装する（図１０（ｂ））。次に、半導体素子ＩＣと基板３１の間にこれらの接合を確保するための封止用の樹脂３７を流し込み、これを硬化させる。

【００４１】この封止用の樹脂３７を流し込むと、半導体素子ＩＣに形成された金バンプＢ３，Ｂ４がその断面が細長い菱形形状の柱型であるために、従来の直方体のバンプＢのように封止用の樹脂３７の流動性が阻害されることがない。したがって、従来のようにペースト状材料の流動性が阻害されることによる気泡Ｋの発生を生じさせることがない。なお、その断面が左右対称の細長い多角形状で幅狭となる部分Ｒ２を有する第４の実施の形態におけるバンプＢ４の場合は、上記第３の実施の形態のものよりも更にスムーズな流れが確保される。

【００４２】（ＭＣＭ実装）次に、複数の半導体素子ＩＣをモジュール化して実装するマルチチップモジュール（以下、ＭＣＭという）に使用する実装について説明する。

【００４３】図１１（ａ）（ｂ）に示すように、複数の半導体素子ＩＣはモジュール基板４１にそれぞれ実装される。この場合は、異方性導電膜（ＡＣＦ）等の導電性を有する接着剤２６を介して実装されＭＣＭが完成する。ここでは、上記金バンプＢ１と配線パターン４５とが導電性を有する接着剤２６を介して接合される。すなわち、本実施の形態のＭＣＭ実装に際しても、ペースト状材料等が半導体素子ＩＣの外周方向にスムーズに流れることにより、気泡Ｋを発生させるようなことがない。その後、ＭＣＭは、他の電子素子４２と共にマザー基板４３に接合される。この場合は、バンプをハンダにより形成して、いわゆるハンダバンプ４４とし、リフローによりハンダバンプ４４を溶融固化させて基板の電極に接続する（従来の第１の方法に対応）。なお、マザー基板４３に接合する際に導電性を有する接着剤２６を使用して接合しても良い。

【００４４】

【発明の効果】本発明に係る半導体素子は、バンプが半導体素子の外周方向に向かって幅狭となる形状と方向性を有するために、ペースト状材料等が半導体素子の外周方向にスムーズに流れるように均一に広がることとなる。したがって、気泡を発生させような事態を生じさせることがなく、しかも、バンプのファインピッチ化を図ることが可能となる。

【００４５】本発明に係る半導体素子が実装された液晶表示装置は、バンプが半導体素子の外周方向に向かって幅狭となる形状を有するために、ペースト状材料等が半導体素子の外周方向にスムーズに流れるように均一に広がることとなる。したがって、ＣＯＧ実装においても、気泡を発生させるような事態を生じさせることがなく、しかも、液晶パネルの一方の基板にかかる荷重を軽減し、接合信頼性の高い半導体素子が実装された液晶表示装置を提供することが可能となる。また、小型化・薄型化が要求されるＣＯＧ実装においてバンプのファインピッチ化を図ることが可能となる。

【００４６】

【図面の簡単な説明】

【図１】本発明の第１の実施の形態の半導体素子を示す図、（ａ）はその平面図、（ｂ）はそのバンプを示す斜視図

【図２】本発明の第２の実施の形態の半導体素子を示す図、（ａ）はその平面図、（ｂ）はそのバンプを示す斜視図

【図３】本発明の第３の実施の形態の半導体素子を示す図、（ａ）はその平面図、（ｂ）はそのバンプを示す斜視図

【図４】本発明の第４の実施の形態の半導体素子を示す図、（ａ）はその平面図、（ｂ）はそのバンプを示す斜視図

【図５】上記各実施の形態の応用例のバンプを示す斜視図

【図６】上記各実施の形態のバンプの形成プロセスを説明する図

【図７】本発明の液晶表示装置の半導体素子の実装構造を示す斜視図

【図８】上記一実施の形態の液晶表示装置を示す断面図

【図９】ＣＯＧ実装の工程を示す断面図

【図１０】一般の半導体素子の実装工程を示す断面図

【図１１】ＭＣＭ実装の例を示す図、（ａ）はその平面図、（ｂ）はその断面図

【図１２】従来の半導体素子の例を示す図

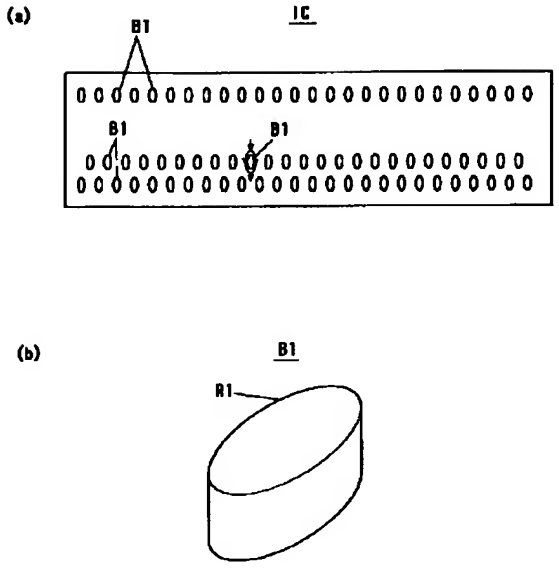
【図１３】従来の半導体素子の例を示す図

【符号の説明】

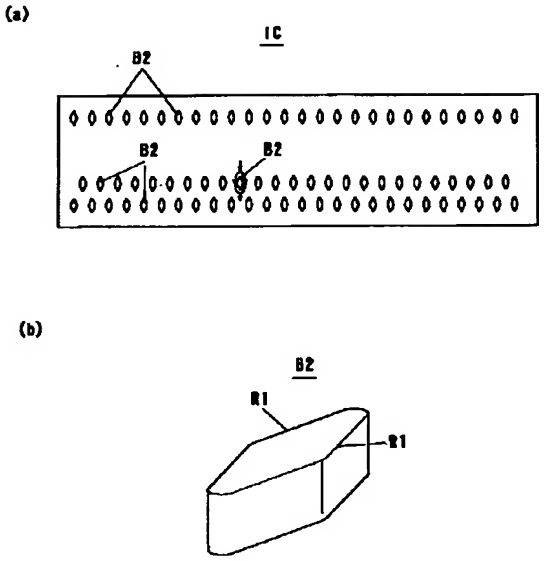
１，３１，４１，４３	半導体実装用の基板、
８	フィルムレジストの開口部、
１１	半導体ウェハ、
２０，３４	配線パターン、
２５	実装領域、
２６，３６	導電性を有する接着剤（ペースト状材料）、
２６ａ	導電性粒子、

37　封止用の樹脂、
B，B1，B2，B3，B4　バンプ、
IC，DrIC　半導体素子、
R1　幅狭の流線形、
R2　細長い多角形状で幅狭となる部分

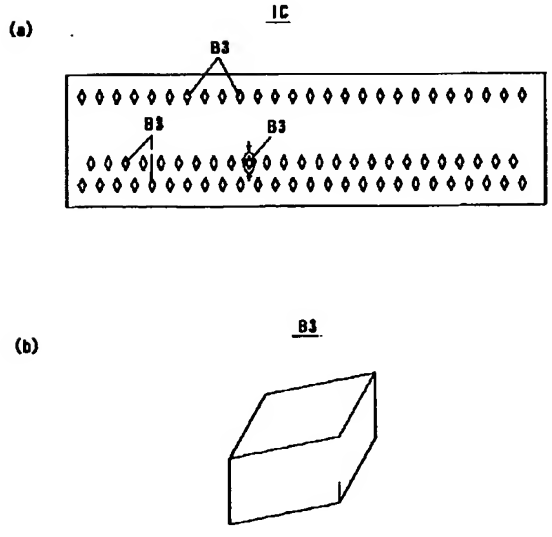
【図1】



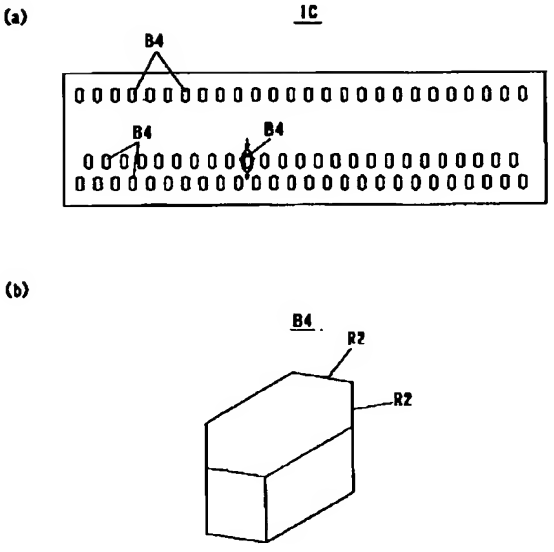
【図2】



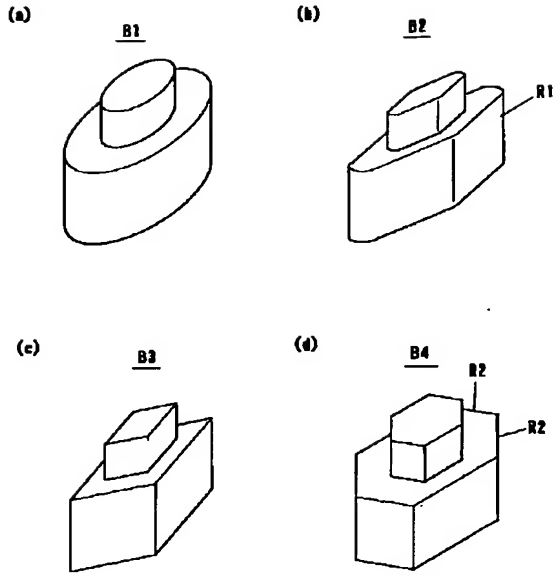
【図3】



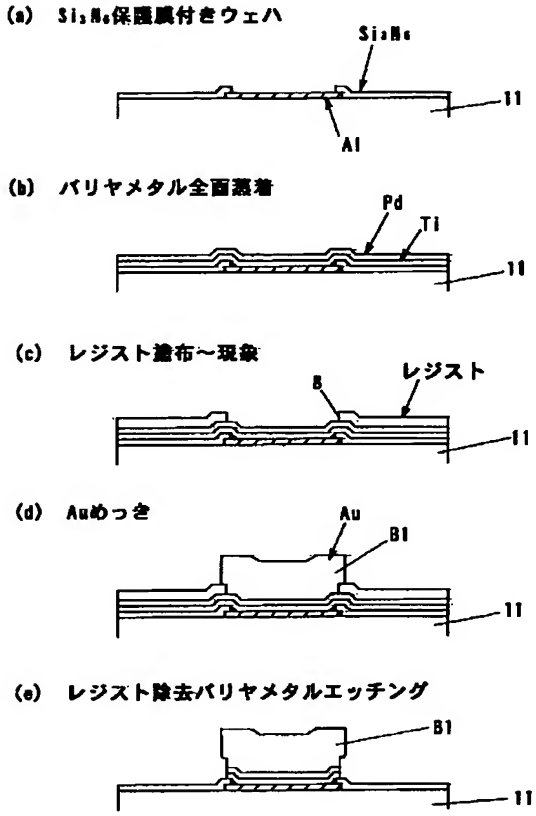
【図4】



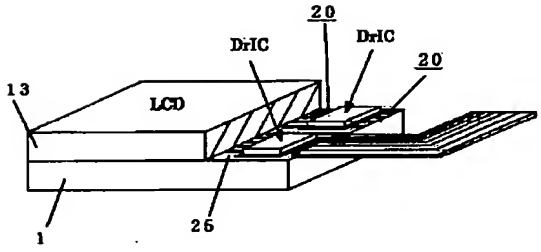
【図5】


(a)
B1
(b)
B2
R1
(c)
B3
(d)
B4
R2
R2

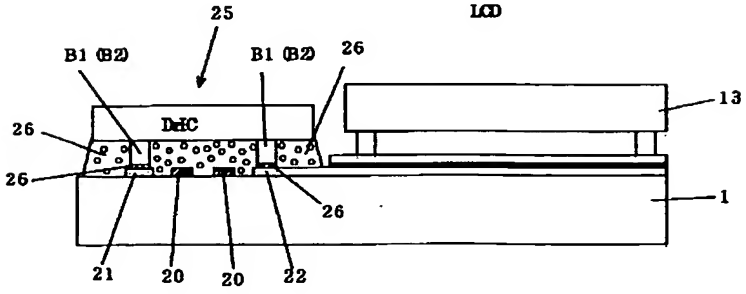
【図6】


(a) Si₃N₄保護膜付きウェハ
Si₃N₄
11
Al
(b) バリヤメタル全面蒸着
Pd
Ti
11
(c) レジスト塗布〜現象
レジスト
11
(d) Auめっき
Au
B1
11
(e) レジスト除去バリヤメタルエッチング
B1
11

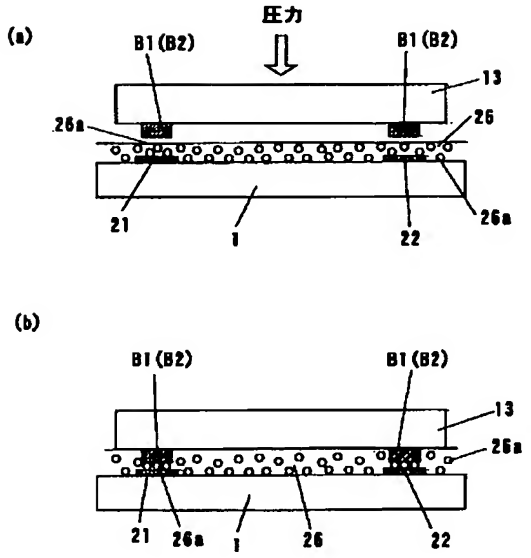
【図7】


20
DrIC
DrIC
20
13
LCD
1
26

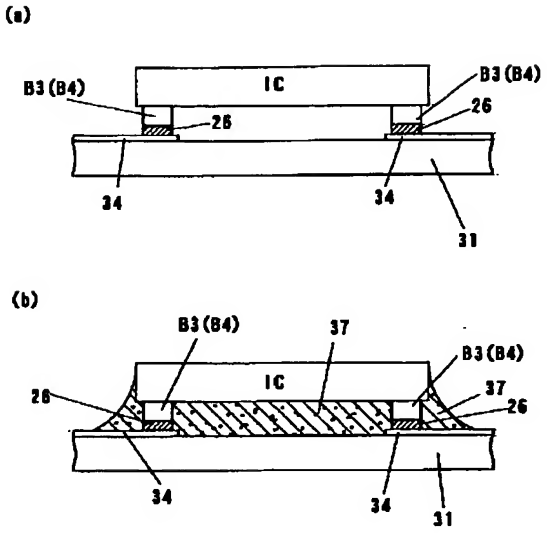
【図8】


25
LCD
B1 (B2)
B1 (B2)
26
13
DrIC
26
26
1
26
21
20
20
22

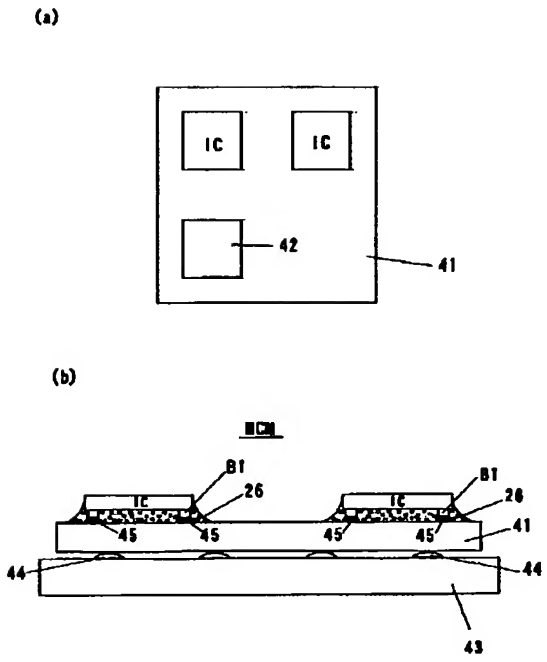
【図9】



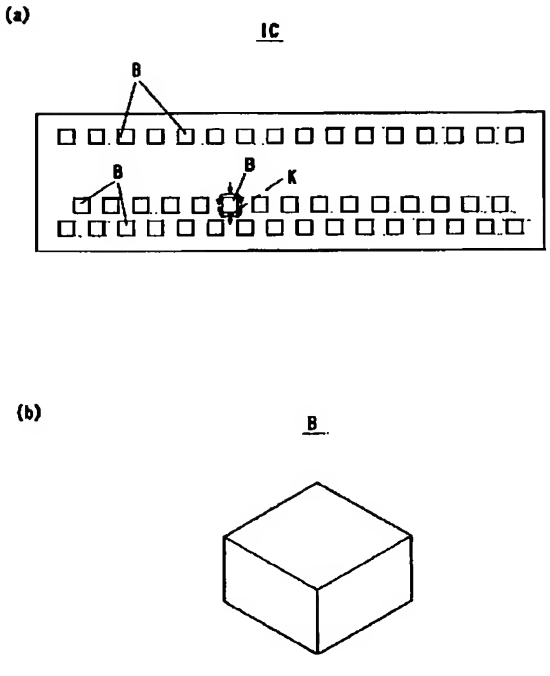
【図10】



【図11】

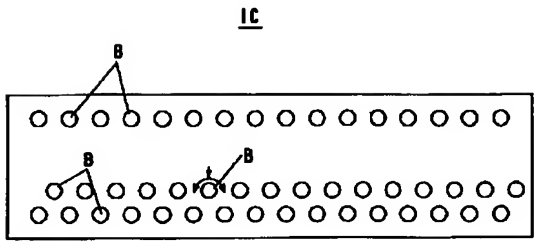


【図12】



【図13】

(a)



(b)